AMENDMENTS TO THE SPECIFICATION

Please delete the section entitled "CROSS-REFERENCE TO RELATED APPLICATIONS" in its entirety and substitute the following section therefor:

CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application claims the benefit of U.S. Provisional Application No. 60/544206, filed on 2/12/2004, which is herein incorporated by reference for all intents and purposes.

[0002] This application is related to the following co-pending U.S. Patent Application, which is filed on the same day as this application, which has a common assignee and at least one common inventor, and which is herein incorporated by reference in its entirety for all intents and purposes:

SERIAL NUMBER	FILING DATE	TITLE
10/816004 (CNTR.2216)	~~HEREWITH~~04/01/2004	FREQUENCY-VOLTAGE MECHANISM FOR MICROPROCESSOR POWER MANAGEMENT

Please delete the section entitled "SUMMARY OF THE INVENTION" in its entirety and substitute the following section therefor:

SUMMARY OF THE INVENTION

[0008] A power management controller for instantaneous frequency-based microprocessor power management according to an embodiment of the present invention includes first and second phase lock loops (PLLs), select logic, and source control logic. The first PLL generates a first core source clock signal at a first frequency based on a bus clock signal. The second PLL generates a second core source clock signal at a programmable frequency based on a frequency control signal and the bus clock signal, where the second PLL generates a lock signal when the second core source clock signal is at a frequency indicated by the frequency control signal. The select logic selects between the first and second core source clock signals to provide a core clock signal for

the microprocessor based on a select signal. The source control logic detects power conditions via at least one power sense signal, provides the frequency control signal according to the power conditions, and provides the select signal. The said source control logic controls the select signal to switch from the first core source clock signal to the second core source clock signal in response to the lock signal.

[0009] The power management controller enables transition from one power state to another in a single clock cycle. The source control logic selects the first core source clock signal while the second PLL is programmed with the second core source clock signal, which is, for example, at a reduced frequency to achieve a reduced power level. Once the second PLL is programmed, the source control logic instructs the select logic to switch to the second PLL. Such transition is significantly faster than that which has heretofore been provided, thus allowing users to benefit from power adjustments without incurring undue delay or performance degradation.

~~**[0010]** The second PLL may be configured to generate a lock signal when the second core source clock signal is at a frequency indicated by the frequency control signal. The source control logic controls the select signal to switch from the first core source clock signal to the second core source clock signal in response to the lock signal.~~ In various embodiments, the first frequency may be associated with the full operating frequency of the microprocessor, whereas the second core source clock signal is programmed to a reduced frequency appropriate for reduced power conditions. The one or more power signals may be provided by any of multiple mechanisms, such as registers, transducers, power signals, etc. The operating system of a computer system may program a register of the microprocessor to indicate a particular reduced power level, where the source control logic reads the programmed register and asserts the frequency control signal accordingly. Temperature transducers and other power signals (e.g., low battery indicators) are contemplated.

[0011] A microprocessor according to an embodiment of the present invention includes a sense interface, a clock source controller, a primary PLL, a programmable PLL, ~~and select logic~~select logic, and at least one internal programmable register. The sense

interface receives at least one power sense signal indicative of power conditions. The clock source controller provides a select signal for switching between first and second core clock signals, provides a core ratio bus indicative of a reduced core clock frequency, and receives a lock signal indicating that the reduced core clock frequency is operative. The primary PLL provides the first core clock signal at a first frequency based on a bus clock signal. The programmable PLL generates the second core clock signal at a frequency based on the core ratio bus and the bus clock signal and provides the lock signal. The select logic selects between the first and second core clock signals to provide a core clock signal based on the select signal. The programmable register is coupled to the sense interface.

[0012] In various embodiments, the sense interface may receive one or more external power sense signals or internal microprocessor signals, such as from programmable registers or the like. The clock source controller determines a reduced power level sufficient to meet the power conditions, and provides the core ratio bus to indicate a core clock frequency to achieve the reduced power level. The clock source controller switches the select signal to select the programmable PLL in response to receiving the lock signal. While the programmable PLL is selected, the clock source controller may switch the select signal back to the primary PLL in response to changes of power conditions.

[0013] A method of instantaneous processor power management according to an embodiment of the present invention includes generating a first source clock at a full power frequency based on a bus clock, generating a second source clock at a reduced power frequency based on the bus clock and a frequency control input, sensing power conditions, and switching between the first and second source clock signals based on sensed power conditions. The sensing includes monitoring at least one power sense signal.

[0014] ~~The method may include monitoring at least one power sense signal.~~ The method may include programming a register to indicate a reduced power level and reading the register. The method may include initially selecting the first source clock signal, providing the frequency control input based on sensed power conditions to indicate the

reduced power frequency, ramping the second source clock signal to the reduced power frequency in response to the frequency control input, providing a lock indication when the second source clock signal achieves the reduced power frequency, and switching to the second source clock signal when the lock indication is provided. The method may further include switching within one bus clock cycle. After switching to the second source clock signal, the method may include sensing a different power condition and switching back to the first source clock signal.